## AMENDMENTS TO THE SPECIFICATION

[0001] This application is a divisional of and claims priority to U.S. Application No. 09/860,031, filed on May 16, 2001, entitled "Layout Technique for Address Signal Lines in Decoders Including Stitched Blocks," which claims priority to U.S. Provisional Application Serial No. 60/204,371, filed on May 16, 2000, ~~and~~ entitled "An Optimal Layout Technique for Row/Column Decoders to Reduce Number of Blocks," the entirety of which are incorporated herein by reference.

[0016] Each generic block 104-107 includes 256 row or column decoders 102, numbered from 0 to 1023 in the decoder block 100. In order to address each decoder 102 individually, each generic block includes address signal lines 112, i.e., address signal lines NB0 - B9, capable of generating a 10-bit address for the 1024 decoders. The signals on lines NB0 - NB9 are the inverse signals of lines B0-B9, respectively. The 10-bit addresses of decoders may be split logically into an 8-bit portion (NB0-B7) to identify the 256 in–block decoder positions, and a 2-bit portion (NB8-B9) to identify the four generic blocks 104-107. The block signal lines NB8-B9 are a subset of the address signal lines NB0-B9. Although Figure 1 is described with reference to signal lines NB0-B9, for simplicity address signal lines NB1-B7 are not shown.

[0017] The block signal lines are NB8-B9 are interleaved such that they switch position between adjacent blocks. The position of lines NB8 and B8 switch between each block. The bottom signal line 120 of the four lines in the NB9/B9 section in a block 104, 105, 106 crosses over the other three lines and switches position to be the top line 122 in the next adjacent block 105, 106, 107, respectively. Also, the NB9 and B9 lines are arranged such that the type of the top signal line 122 in the NB9/B9 section changes in the sequence NB9, NB9, B9, B9 in generic blocks ~~201-204~~ 104-107. With B9=1 and NB9=0, this sequence is [0011].

[0018] Each decoder 102 in the generic block includes block addressing lines 110 representing the two most significant bits of the decoder's 10-bit address. The address signal lines ~~112~~ 111 for each decoder 102 in the generic block are connected to the top signal line in each NB8/B8 and NB9/B9 sections, respectively. With the described layout, each of the generic blocks 104-107 has a different block addresses, [00], [10], [01], and [11], respectively.

[0019] The technique may be expanded to accommodate a larger number of generic blocks. Figure 2 illustrates an exemplary decoder block 200 including five generic blocks 202-206 stitched together to provided 1280 decoders. Each decoder has an 11-bit address, including an 8-bit portion to identify the 256 in-block decoder positions, as described above, and a 3-bit portion to identify the generic block position. The block address signal lines ~~112~~ 110 includes an NB8/B8 section with two block address signal lines, an NB9/B9 section with a four block address signal lines, and an NBa/Ba section, corresponding to the third bit of the block address, with five block address signal lines. Address signal lines in the NBa/Ba section are arranged such that the type of top signal lines 220 changes in the sequence [00001111]. Accordingly, in the five block example, the sequence is [00001] from block 202 to block 206.